AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1-4. (Canceled)

5. (Withdrawn) A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting a corner portion of a transistor portion;

extracting the distance from the corner portion to a line portion;

obtaining the distance where the line portion does not overlap rounding of the corner portion generated after wafer process;

making a correction rule for a correction whether the corner portion is notched or not from the obtained distance; and

obtaining the corresponding relationship between the distance and the intersection part and making a correction based on the correction rule to the corner portion.

6-14. (Canceled)

15. (Currently amended) A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting a correction portion to be corrected from a mask pattern on the mask, the correction portion being an overlapped portion where a line portion overlaps a contact portion;

obtaining a surrounding environment of the correction portion, the surrounding environment of the correction portion being a space width between the line portion and another line portion; and

giving a variable correction amount to the correction portion in accordance with the surrounding environment, the variable correction amount being a line width given to the overlapped portion,

wherein the line width is increased by (i) an integer multiple of a design grid width in accordance with the space width and (ii) a misalignment amount.

16. (Canceled)

17. (Withdrawn) The pattern correcting method according to claim 15, wherein the correction portion is an end portion of a line portion, said line portion overlapping a transistor portion and a portion other than the transistor portion, said end portion being on the portion other than the transistor portion.

18. (Withdrawn) The pattern correcting method according to claim 15, wherein the correction portion is a corner portion of a transistor portion.

19. (Withdrawn) The pattern correcting method according to claim 15, wherein the correction portion is a contact hole portion.

20. (Withdrawn) The pattern correcting method according to claim 15, wherein the correction portion is a contact portion between a via and a line portion.

21. (Withdrawn) The pattern correcting method according to claim 15, wherein the correction portion is a field portion sandwiched between a first transistor portion and a second transistor portion.

22. (Canceled)

23. (Withdrawn) The pattern correcting method according to claim 17, wherein the surrounding environment of the correction portion is the area of the end portion.

24. (Withdrawn) The pattern correcting method according to claim 18, wherein the surrounding environment of the correction portion is the distance between the corner portion and a line portion overlapping the transistor portion and a portion other than the transistor portion.

25. (Withdrawn) The pattern correcting method according to claim 19, wherein the surrounding environment of the correction portion is the difference between

the depth of a contact hole correspondence to the contact hole portion and that of another contact hole.

26. (Withdrawn) The pattern correcting method according to claim 20, wherein the surrounding environment of the correction portion is the distance between the contact portion and the end of the line portion closer to the contact portion.

27. (Withdrawn) The pattern correcting method according to claim 21, wherein the surrounding environment of the correction portion is the width of the field portion sandwiched between the first transistor portion and the second transistor portion.

28. (Canceled)

29. (Previously presented) The pattern correcting method according to claim 28, wherein the line width is further increased by half the design grid width.

30. (Withdrawn) The pattern correcting method according to claim 23, wherein the variable correction amount is a fringe amount to be added to the end portion, and the fringe amount is increased by an integral multiple of a design grid width in accordance with the area of the end portion.

31. (Withdrawn) The pattern correcting method according to claim 30, wherein the fringe amount is further increased by half the design grid width and/or an alignment margin.

32. (Withdrawn) The pattern correcting method according to claim 24, wherein the variable correction amount is a presence/non-presence of a notch formed in the corner portion, and whether the notch is formed or not is determined in accordance with the distance between the corner portion and the line portion.

33. (Withdrawn) The pattern correcting method according to claim 32, wherein the distance between the corner portion and the line portion is reduced by an alignment margin.

34. (Withdrawn) The pattern correcting method according to claim 25, wherein the variable correction amount is a bias amount added to the contact hole portion, and the bias amount is increased by an integral multiple of a design grid width in accordance with the difference between the depth of the contact hole correspondence to the contact portion and that of said another contact hole.

35. (Withdrawn) The pattern correcting method according to claim 34, wherein the bias amount is further increased half the design grid width.

36. (Withdrawn) The pattern correcting method according to claim 34, wherein the difference between the depth of the contact hole correspondence to the contact hole portion and that of said another contact hole is the thickness of a gate.

37. (Withdrawn) The pattern correcting method according to claim 25, wherein the variable correction amount is a bias amount added to the contact hole, and the bias amount is increased by an integral multiple of a design grid width in accordance with the difference between the depth of the contact hole correspondence to the contact hole portion and that of said another contact hole.

38. (Withdrawn) The pattern correcting method according to claim 37, wherein the bias amount is further increased by half the design grid width.

39. (Withdrawn) The pattern correcting method according to claim 37, wherein the difference between the depth of the contact hole correspondence to the contact hole portion and that of said another contact hole is the thickness of a gate.

40. (Withdrawn) The pattern correcting method according to claim 26, wherein the variable correction amount is a fringe amount added to the contact portion, and the fringe amount is increased by an integral multiple of a design grid width in accordance with the distance between the contact portion and the line portion.

41. (Withdrawn) The pattern correcting method according to claim 40, wherein the fringe amount is increased by half the design grid width and/or an alignment margin.

42. (Withdrawn) The pattern correcting method according to claim 27, wherein the first transistor portion includes a first contact portion, and the second transistor portion includes a second contact portion;

a fringe amount of the first contact portion and that of the second contact portion are enlarged by a minimum design rule; and

the variable correction amount corresponds to the width added to the field portion sandwiched between the first transistor portion and the second transistor portion, and the width is increased by an integral multiple of a design grid width in accordance with the enlarged first and second contact portions.

43. (Canceled)

44. (Previously presented) The pattern correcting method according to claim 29, wherein the line width is further increased by a misalignment amount.

45. (New) A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting a correction portion to be corrected from a mask pattern on the mask, the correction portion being an overlapped portion where a line portion overlaps a contact portion;

obtaining a surrounding environment of the correction portion, the surrounding environment of the correction portion being a space width between the line portion and another line portion; and

giving a variable correction amount to the correction portion in accordance with the surrounding environment, the variable correction amount being a line width given to the overlapped portion,

wherein the line width is increased by (i) an integer multiple of a design grid width in accordance with the space width, (ii) a misalignment amount, and (iii) half the design grid width.